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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	**Confirmation No.**
Kazuto NISHIDA	:	Atty Docket 00177/526327
Serial No. 09/331,763	:	Group Art Unit 3727
Filed June 25, 1999	:	Examiner J. Merek
METHOD AND APPARATUS FOR MOUNTING ELECTRONIC COMPONENT ON CIRCUIT BOARD	:	

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PATENT OFFICE FEE TRANSMITTAL FORM

Assistant Commissioner for Patents,
Washington, DC 20231

Sir:

Attached hereto is a check in the amount of $180.00 to cover Patent Office fees relating to filing the following attached paper:

Information Disclosure Statement $180.00

A duplicate copy of this paper is being submitted for use in the Accounting Division, Office of Finance.

The Commissioner is authorized to charge any deficiency or to credit any overpayment associated with this communication to Deposit Account No. 23-0975, with the EXCEPTION of deficiencies in fees for multiple dependent claims in new applications.

Respectfully submitted,

Kazuto NISHIDA

By _____
Joseph M. Gorski
Registration No. 46,500
Attorney for Applicant

THE COMMISSIONER IS AUTHORIZED TO CHARGE ANY DEFICIENCY IN THE FEES FOR THIS PAPER TO DEPOSIT ACCOUNT NO. 23-0975

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INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents,
Washington, DC 20231

Sir:

Pursuant to the provisions of 37 CFR 1.56, 1.97 and 1.98, Applicant requests consideration of [X] the references listed on attached form PTO-1449 and/or [] the additional information identified below in paragraph 3. A legible copy of each reference listed on the form PTO-1449 and each U.S. patent application listed below is enclosed, except a copy is not provided for each reference previously cited by or submitted to the Patent Office in prior parent application Serial No.

1a. [] This Information Disclosure Statement is submitted:

within three months of the filing date (or of entry into the National Stage) of the above-entitled application, **or**

before the mailing of a first Office Action on the merits or the mailing of a first Office Action after the filing of an RCE,

and thus no certification and/or fee is required.

1b. [X] This Information Disclosure Statement is submitted

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after the events of above paragraph 1a and prior to the mailing date of a final Office Action or a Notice of Allowance or an action which otherwise closes prosecution in the application, and thus:

(1) [] the certification of paragraph 2 below is provided, **or**

(2) [X] the fee of $180.00 specified in 37 CFR 1.17(p) is enclosed.

1c. [] This Information Disclosure Statement is submitted:

after the mailing date of a final Office Action or Notice of Allowance or action which otherwise closes prosecution in the application, and prior to payment of the issue fee, and thus:

the certification of paragraph 2 below is provided, and

the fee of $180.00 specified in 37 CFR 1.17(p) is enclosed.

2. It is hereby certified

a. [] that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Statement, or

b. [] that no item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any individual designated in §1.56(c) more than three months prior to the filing of the Statement.

3. [] Consideration of the following list of additional information (including any copending or abandoned U.S. application, prior uses and/or sales, etc.) is requested.

4. For each non-English language reference listed on the attached form PTO-1449, reference is made to:

a. [X] a full or partial English language translation set forth below,

b. [X] a foreign patent office search report (in the English language) submitted herewith,

c. [] the concise explanation contained in the specification of the present application at page,

d. [] the concise explanation set forth in the attached English language abstract,

e. [] the concise explanation set forth below or on a separate sheet attached to the reference:

Japanese Unexamined Patent Publication No. 5-206208 issued on August 13, 1993

In column 4, lines 27-39, it is described that " [0010] [Working Example] In a sectional view of Fig. 1, the projection electrodes of a semiconductor chip are arranged with 100μm-square, 25μm-height, and 30μm-gap at their tip areas. The thickness of conductive particle after circuit connection in a sectional view of Fig. 3 is 2μm, the projection electrode height is 22μm, the circuit electrode height is 0.2 μm. In such a case, a circuit connection example will be described when a particle-shifted type anisotropic conductive film having a thickness shown in Table 1 is used. The projection electrode of the semiconductor chip is made of gold, a surface of polystyrene nucleus of conductive particle is subjected to gold-plating, and a circuit and electrodes of a glass circuit board are subjected to gold-plating. As an insulating adhesive agent layer, epoxy adhesive including latent curing agent was used."

In column 5, lines 21-25, it is described that "Now, as shown in Fig. 1, the projection electrodes of the semiconductor chip are aligned with the circuit electrodes, and the semiconductor chip is fixed through bonding with heating of 190°C for 20 seconds while applying a pressure of 50 gf/electrode".

Japanese Unexamined Patent Publication No. 62-188184 issued on August 17, 1987

On page 9, upper right column, lines 2-15, it is described that

"(2) Film formation

This adhesive composition is applied on a separator (a silicone-processed polyester film) by using a bar coater, dried with 100°C for 5-30 minutes depending on its thickness to remove its solvent for forming an adhesive film".

(3) Evaluation

the above adhesive film cut to have 3mm-adhesive width and 100mm-length is placed onto a flexible circuit board (FPC) having 0.1mm-line width, 0.2mm-pitch, and 35μm-thickness circuit

and having the 100mm-whole circuit width and then temporarily bonded thereto with heat of 120°C and pressure of 10kg/cm^2 for 5 seconds for obtaining a FPC having an adhesive member.".

On page 9, lower right column, lines 3-5 from the bottom, it is described that "Au-coating atomized Ni spheres, Ag-coating glass spheres, and solder spheres each having 150°C-melting point as conductor particles are used." for reference examples.

Japanese Unexamined Patent Publication No. 4-280443 issued on October 6, 1992

In claim 1, it is described that "a method of performing electrical and mechanical interconnection between an electrical component and a component placement board, the method comprising steps of: providing a board having a metallized pattern; providing an electric component having solder bumps thereat; adding an adhesive material including a flux material to the board or the component; and positioning the component onto the board; reflowing the solder bumps, wherein the flux material promotes adhesion of the solder to the board metallized pattern and the cured adhesive material performs mechanical interconnection between the board and the component.".

Japanese Unexamined Patent Publication No. 4-351863 issued on December 7, 1992

In the third paragraph of claim 1, it is described that "a method of manufacturing a conductor member, comprising steps of (1) forming an adhesive layer; (2) bringing a mask into close contact with a surface of the adhesive layer with the mask having a through hole at its necessary portion; "(3) irradiating a laser beam through the through hole of the mask, and thereby forming a hole at least a part of the adhesive layer in its thickness direction; (4) arranging conductive particles into the hole from the through hole of the mask; and removing the mask from the surface of the adhesive layer.".

"Bare Chip Mounting centering COB and TOB mounting--latest technology development and reliability measures--" issued on January 31, 1990 by Gijutsu Joho Kyokai (English translation of Fig. 14 attached to Form PTO-1449)

On page 46, lines14-24, it is described that "In an example shown in Fig. 14 (Seico Epson), instead of a metal particle as a conductive particle, a ϕ7.5μ-spherical resin (divinyl benzene copolymer) which is subjected to about 500A-Au-plating is used (Fig. 14(a)). This Au-plating plastic spheres are mixed with an adhesive to become in paste, and then the paste is printed and coated on board electrodes and simultaneously, an epoxy adhesive is coated on a position where an IC chip is placed (Fig. 14(b)). The IC chip having Al electrodes (bumpless chip) is aligned onto the board with the IC chip in a face down state and then pressure and heating is applied to them for adhesion and curing, resulting in connection (Fig. 14(c))."

Japanese Unexamined Patent Publication No. 7-321148 issued on December 8, 1995

In claim 1, it is described that

"[Claim 1]

A semiconductor device mounting method of mounting a face-down semiconductor device having a projection contacts onto a circuit board using a conductive adhesive, the method comprising steps of:

forming a coating film of a conductive thermoplastic adhesive on a support substrate;

bringing the projection contacts of the semiconductor device into contact with the coating film of the adhesive on the support substrate while heating the conductive adhesive on the support substrate to maintain its plastic state, resulting in transfer of the conductive adhesive onto the contacts;

bringing the projection contacts of the semiconductor device into contact with the connection electrodes of the circuit board while maintaining a plastic state of a transfer part of the conductive adhesive formed in the previous step; and

cooling the conductive adhesive while bringing the projection contacts of the semiconductor device into contact with the connection electrodes of the circuit board, resulting in adhesion between them."

Japanese Unexamined Patent Publication No. 6-37144 issued on February 10, 1994

In column 2, lines 24-28, it is described that "2) Although a method of using an ultrasonic as well as an applying force 7 together as one means of the means for solving an issue may be conceived as an application of the prior art, it is necessary to arrange an ultrasonic generating device having a large capacity in proportion to increasing of the number of pins of the semiconductor element 1, resulting in increasing the cost."

Japanese Unexamined Patent Publication No. 8-88462 issued on April 2, 1996

In claims 1 and 3, it is described that "[Claim 1] A method of mounting a semiconductor device using an anisotropic conductive film, the method comprising: (a) a step of aligning a semiconductor device sucked with a heat tool with an anisotropic conductive film having a base film and an anisotropic conductive layer; (b) a step of moving downward the semiconductor device and pressurizing and heating the anisotropic conductive film between the semiconductor device and a transfer stage having a cushion member at its surface arranged below the anisotropic conductive film; (c) a step of moving upward the heat tool to separate the below the anisotropic conductive layer from the base film and then transferring the below the anisotropic conductive layer on the semiconductor element; and (d) a step of conveying the heat tool and mounting, onto a position to be mounted, the semiconductor device on which the below the anisotropic conductive layer has been transferred." and

"[Claim 3] An apparatus for mounting a semiconductor device using an anisotropic conductive film, characterized in that (a) an anisotropic conductive film having a base film and an anisotropic conductive layer and looped over a freed reel and a winding reel; (b) a transfer stage arranged below the anisotropic conductive film and having a cushion member at its surface; (c) a

semiconductor device tray, arranged in the vicinity of the transfer stage, for accommodating semiconductor devices; and (d) a mounting stage arranged in the vicinity of the transfer stage and setting a semiconductor device mounting body onto which the semiconductor device should be mounted theronto are arranged, and (e) the semiconductor device accommodate in the semiconductor device tray is sucked with the heat tool and conveyed onto the anisotropic conductive film, and thereafter, the heat tool is moved downward to separate the anisotropic conductive layer from the base film and transfer the anisotropic conductive layer onto the semiconductor device due to the cooperation with the transfer stage, and then the heat tool is conveyed to mount the semiconductor device onto the semiconductor device mounting body set on the mounting stage."

5. [X] A foreign patent office search report citing one or more of the references is enclosed.

Respectfully submitted,

Kazuto NISHIDA

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